REMARKS

Applicants respectfully request favorable reconsideration of this application, as amended.

The specification has been revised to correct the informalities noted by the Examiner.

Claims 1 and 5-8 were examined as a result of Applicants' earlier election of species. By this Amendment, Claims 1 and 6-7 have been cancelled without prejudice or disclaimer. Claims 5 and 8 have been amended and are allowable as discussed below. New Claims 31-37 have been added, dependent from Claim 5, and are also allowable. Non-elected Claims 2-4 and 9-30 have been cancelled, without prejudice or disclaimer, in view of the Allowability of Claims 5, 8, and 31-37, so that this application may be passed to issue.

In the outstanding Office Action, Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over either of Kamagaki (6,531,735) or Horiguchi (6,815,759) in view of Jones (6,531,731). Claim 8 was rejected under 35 U.S.C. § 102(e) as being anticipated by Horiguchi. As presently amended, however, each of Claims 5 and 8 distinguishes patentably from the applied references.

Claim 5, for example, recites a semiconductor memory element comprising a well region having a first conductivity

type and formed in a principal surface of a semiconductor substrate. Source and drain regions each having a second conductivity type are formed in the well region to have a specified distance therebetween. First and second gates and first and second charge storage regions are formed, via a first insulating film, on a portion of the principal surface of the semiconductor substrate between the source and drain regions. A third gate is formed over the charge storage regions via a second insulating film, the first and second charge storage regions being provided between said first and second gates. Further, each of the first and second charge storage regions has a layer composed of stacked semiconductor nano-crystals.

It is apparent that amended Claim 5 distinguishes patentably from, Kamigaki, Horiguchi, and Jones, at least in that none of the applied references teaches a memory element having the claimed arrangement of first and second storage regions, each having a layer composed of stacked semiconductor nano-crystals. While it is noted that Jones discloses the use of nano-crystals, the reference fails to teach an arrangement in which the nano-crystals are stacked, as particularly claimed. Accordingly, Jones would not have suggested modifying either of, Kamigaki or Horiguhchi in such a manner as would be necessary to achieve Applicants'

invention as set forth in amended Claim 5.

Claim 8, as amended, recites a semiconductor memory element comprising a well region having a first conductivity type and formed in a principal surface of a semiconductor substrate. Source and drain regions each having a second conductivity type are formed in the well region to have a specified distance therebetween. First and second gates and first and second charge storage regions are formed, via a first insulating film, on a portion of the principal surface of the semiconductor substrate between the source and drain regions. A third gate is formed over the charge storage regions via a second insulating film, the first and second charge storage regions being provided between the first and second gates. Further, each of the first and second charge storage regions has a respective floating gate composed of polysilicon.

As to Horiguchi, Applicants would respectfully note that the reference does not teach a structure having first and second charge storage regions <u>each having a respective gate</u>, as set forth in Claim 8. Rather, Horiguchi discloses a single floating gate arrangement.

Accordingly, Claim 8 distinguishes patentably from Horiguchi.

For the reasons discussed above, Applicants

respectfully urge that the outstanding rejections be withdrawn and that this application now be passed to issue.

The Commissioner is hereby authorized to charge to deposit Account No. 50-1165 any fees that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on November 14, 2005.

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Mitchell W. Shapiro